

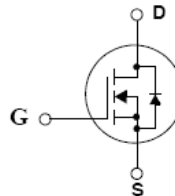
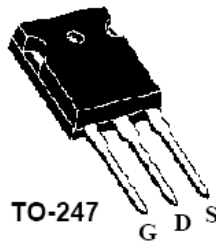
1 Description

These N-Channel enhancement mode power field effect transistors are produced using planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

2 Features

- 60V / 84A, $R_{DS(on)} = 13m\Omega$ (typ) @ $V_{GS} = 10V, I_D = 39A$
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability..



3 Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	apQ65SN06AD	Units
V_{DSS}	Drain-Source Voltage	60	V
I_D	Drain Current - Continuous ($T_C = 25^\circ C$) - Continuous ($T_C = 100^\circ C$)	65	A
		39	A
I_{DM}	Drain Current – Pulsed ①	260	A
V_{GS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy ②	650	mJ
I_{AR}	Avalanche Current	65	A
E_{AR}	Repetitive Avalanche Energy	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③	7.0	V/ns
P_D	Power Dissipation ($T_C = 25^\circ C$) - De-ate above $25^\circ C$	150	W
		1.0	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	soldering temperature for 10 seconds	300	$^\circ C$

* note :

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 30V$, starting $T_J = 25^\circ C$, $L = TBD$, $R_G = 0\Omega$, $I_{AS} = 65A$
- ③ $I_{SD} \leq 65A$, $di/dt \leq 100A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ C$.



DEVICE SPECIFICATION

apQ65SN06AD

60V/65A N-Channel MOSFET

4 Thermal Characteristics

Symbol	Parameter	apQ65SN06AD		Units
		Typ.	Max.	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	1.0	$^{\circ}\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^{\circ}\text{C}/\text{W}$

5 Electrical Characteristics $T_C = 25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}$, Referenced to 25°C	--	0.07	--	$\text{V}/^{\circ}\text{C}$
I_{DSS}	Gate to Source leakage current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	--	--	25	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 39\text{ A}$ ④	--	13	16	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 32.5\text{ A}$ ①	--	--	100	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	2003	--	pF
C_{oss}	Output Capacitance		--	449	--	pF
C_{rss}	Reverse Transfer Capacitance		--	32.5	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 39\text{ A}, R_G = 4.7\ \Omega, R_D = 0.77\ \Omega, V_{GS} = 10\text{ V}$ ④	--	11.3	--	ns
t_r	Turn-On Rise Time		--	32.4	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	41	--	ns
t_f	Turn-Off Fall Time		--	11.9	--	ns
Q_g	Total Gate Charge	$V_{DS} = 30\text{ V}, I_D = 39\text{ A}, V_{GS} = 10\text{ V}$ ④	--	36.1	--	nC
Q_{gs}	Gate-Source Charge		--	7.6	--	nC
Q_{gd}	Gate-Drain Charge		--	11.7	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	65	--	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	260	--	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 32.5\text{ A}$	--	--	1.5	V



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t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = 39\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$ ④	--	50.8	--	ns
Q_{rr}	Reverse Recovery Charge		--	80.6	--	μC

Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 30\text{ V}$, starting $T_J = 25^\circ\text{C}$, $L = \text{TBD}$, $R_G = 0\Omega$, $I_{AS} = 65\text{ A}$
- ③ $I_{SD} \leq 65\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$. Depend on FT Test.
- ⑤ CP Test



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60V/65A N-Channel MOSFET

Note

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